DESIGN AND IMPLEMENTAION OF A DDR SDRAM CONTROLLER FOR SYSTEM ON CHIP

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Contents

• Double Data Rate Interfaces
• DDR SDRAM Architecture and Functionality
• DDR Memory Controller
• Data Resynchronization
• Floorplan and Place & Route
• Future Work
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Double Data Rate Interfaces

New
- Data Transmissions on rising and falling edge
- Data Strobe

Advantages
- Time of Flight
- Clock Skew
- Pin Count
- Bandwidth

Disadvantage
- Synchronization
SDRAM Architecture

- Four Banks
- Row and Column Select Lines
- 1T Memory Cells
- Sense Amplifiers
- Global Data Path
DDR SDRAM Architecture

- 2n-prefetch
- Delay Lock Loop
DDR SDRAM Improvements

- Long Delay in Column Decode and Data Lines
- Added a Delay Lock Loop to Increase Clock Frequency
DDR SDRAM Commands

Same Commands as for Standard SDRAM
• READ
• WRITE
• ACTIVATE
• PRECHARGE
• REFRESH
• MRS (Mode Register Set)
Added
• EMRS (Extended MRS)
DDR SDRAM Memory Controller
Core Memory Controller

Diagram:
- Initialize
- Address
- Next Address
- Open Banks
- Current Address
- Command
- Increment Boundary
- Read Write Command
- Row Open
- Activate/Precharge Command Address
- Refresh
- Read/Write Command Address
- Command Timing
- Command Address
- Enable DQS
AHB Interface
Arbiter

![Diagram of Arbiter](image_url)
Capturing the Data

- Phase Shift the Data Strobe
- Resynchronize the Data

![Waveform diagram showing Clk, Command, Address, Data Strobe, and Data with 'Don’t care' shaded areas.](image-url)
Phase Shift the Data Strobe

- Delay Lock Loop
- Inverter Delay
- PCB Line Delay
- Programmable Delay Line with Temperature Sensing
Synchronization of the Data

One Flip-Flop for each Flank to Sample

Data Strobe

Data

Data Even

Data Odd

Do not care
Synchronization of the Data Continued

Reference Clock Low

Reference Clock High

Data Strobe
Reference Clk
Clk x2
Data Even

Rising Edge of Data Strobe

Data Stable

Not stable
Synchronization of the Data Continued

Simplified Phase Detector

Clk I

Clk II

High

D Q I

&

S Q

R

Phase

Clk II

High

D Q II

Q I

Q II

Phase

Undefined
Floorplan

AHB I Read, Write and Address Buss

AHB I Control Signals
Clock Signals
APB Signals

AHB II Control Signals

AHB II Read, Write and Address Buss

DDR Memory Controller

DDR Control Signals
Address and Data Buss

Data Buffer (AHB I)

Data Buffer (AHB II)

AHB Interface region
Place & Route
Future Work

• Improved Refresh Handling
• Attempt to Reduce Initial Latency for Bursts
• Improved Buffer Handling
Conclusion

• Working Implementation
• Smaller Changes to Improve Performance
• Highlights Difficulties and Solutions
Questions ?